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VDP-7 Raster / Vector Display Processor

Technical Data Sheet

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High-performance display processor for technical visualization systems

The VDP-7 combines line-oriented technical graphics acceleration with raster framebuffer operations, programmable display timing, hardware cursor support and a 32-bit host programming interface. It is intended for engineering visualization, instrumentation, simulation and specialized OEM display systems.

Document Status and Product Notice

Status

This data sheet describes VDP-7 production silicon Revision B1/B2 and later compatible revisions. Programming behavior is defined in RM-VDP7-03.

Qualification

Electrical and timing limits apply at the device pins under the stated operating conditions. Board-level limits may be narrower because of memory, RAMDAC, clock and signal-integrity constraints.

Availability

VDP-7 is a CURRENT Sinneslöschen display product. Industrial-temperature screening is available for qualified OEM programs.

APPLICATION NOTE

Do not infer a qualified display mode solely from register programmability. Pixel clock, framebuffer bandwidth, RAMDAC limits and board layout must all be qualified together.

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Features and Applications

Principal Features

VDP-7 is optimized for technical displays where deterministic drawing, high-resolution timing and long product support are more important than consumer multimedia functions.

Typical Applications

Engineering workstations, instrumentation displays, laboratory visualization, industrial terminals, simulation systems and custom OEM display controllers.

Feature	Summary
Host Interface	32-bit memory-mapped host interface; posted command writes supported on qualified host bridges.
Command FIFO	64 x 32-bit word hardware FIFO with programmable low-water interrupt.
Framebuffer	External 64-bit framebuffer interface; indexed 8-bit, RGB565 and XRGB8888 storage formats.
Geometry	Hardware line/polyline generation, rectangles and filled polygon edge processing with 16.8 fixed-point coordinates.
Raster Operations	Sixteen logical ROP functions, constant fill, source copy, destination read/modify/write and transparent source modes.
Display Timing	Programmable horizontal/vertical timing; external RAMDAC/clock subsystem; qualified pixel clocks to 135 MHz board-dependent.
Cursor	64 x 64 hardware cursor with transparent states and two programmable colors.
Interrupts	Command completion, FIFO low, vertical blank, error and diagnostic interrupt sources.

Functional Architecture

Overview

The device separates host command acceptance, geometric setup, raster/ROP execution, framebuffer scheduling and display scanout. The scanout path receives arbitration priority sufficient to maintain programmed timing when the external memory subsystem meets qualified bandwidth requirements.

Data Path

Register, command and core pixel operations use a 32-bit internal data path. The external framebuffer interface is 64 bits wide and may be organized by the board designer using qualified SDRAM or synchronous graphics memory arrangements.

VDP-7 FUNCTIONAL BLOCK DIAGRAM



Display scanout shares the external framebuffer scheduler with rendering traffic.

Host Interface

Programming Model

The host sees a 4 KB memory-mapped control aperture, a write-only command port and implementation-specific framebuffer windows. Register and command words are 32 bits.

Ordering

Posted command writes are permitted on qualified bridges. Software must use FIFO_STATUS or another documented ordering read before reclaiming host command buffers.

Parameter	Value	Notes
Host data width	32 bits	Memory-mapped registers and command writes
Register aperture	4 KB	Naturally aligned 32-bit registers
Host clock	Up to 33 MHz	Qualified local-bus implementation
Posted writes	Supported	Ordering read required
Byte order	Board-defined	Driver performs any required swapping

Command Processor and FIFO

Command Submission

A 64-word FIFO decouples host writes from geometry and raster execution. Fixed and variable-length packets are decoded into rendering operations and state changes.

Watermarks

FIFO low-water status can generate an interrupt. Software should submit commands in batches large enough to reduce host overhead without starving other clients.

Item	Value	Description
FIFO depth	64 words	32-bit command words
Watermark	Programmable	Interrupt/status threshold
Packet alignment	32-bit	No byte-granular packets
Completion	Marker/idle	FIFO empty does not imply raster idle

Framebuffer Interface

Interface

The VDP-7 provides a 64-bit external framebuffer interface with separate address/control signals and board-qualified burst access. The controller arbitrates display fetches, drawing writes, destination reads and selected command DMA activity.

Bandwidth

Required bandwidth depends on pixel clock, stored bytes per pixel and rendering traffic. Display scanout receives priority, so rendering throughput decreases as scanout demand approaches available memory bandwidth.

Parameter	Typical	Notes
Interface width	64 bits	External framebuffer data
Memory clock	40-66 MHz	Board qualified
Peak raw bandwidth	320-528 MB/s	Before protocol overhead
Address granularity	Byte	Software-visible addresses
Preferred alignment	32 bytes	For burst-friendly surfaces

APPLICATION NOTE

A 110 MHz XRGB8888 scanout requires approximately 440 MB/s of raw pixel fetch bandwidth before memory protocol overhead. Qualify such modes only on boards designed for the required sustained bandwidth.

Drawing Engine

Geometry

The drawing engine accepts signed 16.8 fixed-point coordinates for operations supporting subpixel positioning. Origin, scale and rectangular clip state are applied before rasterization.

Raster Operation Unit

Sixteen logical ROP functions combine source, pattern and destination data. Destination-read operations consume additional memory bandwidth and may reduce throughput.

Operation	Hardware Support
Point / span	Yes
Line / polyline	Yes; subpixel endpoints
Filled rectangle	Yes
Filled convex polygon	Yes
General polygon edge list	Supported through command packets
Source blit	Yes
Pattern fill	Yes
Host image upload	Yes, packetized

Line and Polyline Operations

Line Setup

Endpoint coordinates use 16.8 fixed-point values. Hardware performs clipping and incremental edge generation. Endpoint suppression is available for connected polylines.

Performance

Throughput depends on line length, pixel format, ROP, destination-read requirements and framebuffer contention. Short independent segments are command-overhead limited; long segments are raster/memory limited.

Function	Capability	Notes
Subpixel endpoint	1/256 pixel	16.8 fixed-point
Clipping	Rectangular	Before pixel generation
Width	1 pixel core	Wider lines generated by library
Pattern/stipple	Supported	Programmable mask
ROP	16 functions	Per stored pixel word

Polygon and Rectangle Operations

Rectangles

Axis-aligned rectangles may be emitted as a dedicated fill command. This path minimizes geometry setup overhead and is preferred for window clearing and solid UI regions.

Polygons

Filled polygon commands provide edge setup and span generation for technical graphics. Extremely complex concave objects should be tessellated by host software or Graphics Library 4.1.

Parameter	Limit / Behavior
Coordinate range	-32768 to +32767 integer pixels plus 8 fractional bits
Clip rectangle	Programmable independent X/Y bounds
Fill rule	Even-odd for general polygon packets
Maximum vertices	Packet dependent; see RM-VDP7-03
Degenerate edges	Ignored or reduced per command definition

Blit and Raster Operations

Blit Engine

The blit path supports source copy, constant fill, overlapping moves and selected transparent-source operations. Direction controls permit safe movement of overlapping rectangles.

ROP Behavior

ROP logic operates on stored pixel words before RAMDAC conversion. In indexed mode, operations affect palette indices rather than post-DAC RGB values.

Operation	Support	Notes
Constant fill	Yes	Fast path
Source copy	Yes	Burst optimized
Overlap safe copy	Yes	Direction controlled
Transparent source	Selected	Format dependent
Destination ROP	Yes	Consumes read bandwidth
Host upload	Yes	Command packet data

Clipping and Scaling

Clipping

A programmable rectangular clip is applied after origin and scale state. Off-screen surfaces may use clip bounds independent of the active display dimensions as long as framebuffer address limits remain valid.

Scaling

Programmable coordinate scale factors support viewport-style transformations for technical applications. Graphics Library 4.1 normally manages scale state for application software.

State	Description
Origin X/Y	Signed translation applied before clipping
Scale X/Y	Fixed-point coordinate scale
Clip min/max	Inclusive/exclusive bounds per programming reference
Framebuffer limit	Independent address safety bound
Surface pitch	Programmed in bytes

Pixel Formats

Stored Formats

VDP-7 supports indexed and packed RGB framebuffer storage. RAMDAC and board implementation determine the physical analog output format.

Color Interpretation

ROP and blit operations act on stored pixel words. Palette lookup is used for indexed-color scanout; packed RGB modes bypass indexed lookup for normal scanout.

Format	Bits/Pixel	Storage	Use
INDEX8	8	1 byte	Technical palettes, low bandwidth
RGB565	16	2 bytes	Direct color, moderate bandwidth
XRGB8888	32	4 bytes	High-quality direct color
MONO8	8	1 byte	Diagnostic/luminance use

Display Timing

Timing Generator

Horizontal and vertical totals, active intervals, blanking and sync positions are fully programmable within device register ranges. Pixel clock generation and analog conversion are external to the core.

Qualification

A representable timing is not automatically a qualified timing. Verify RAMDAC clock limit, memory bandwidth, analog signal integrity and monitor requirements.

Parameter	Range	Notes
Horizontal total	256-4096 clocks	Board granularity may apply
Horizontal active	Up to 2048 pixels	Qualified mode may be narrower
Vertical total	200-2048 lines	Progressive scan
Vertical active	Up to 1600 lines	Qualified mode may be narrower
Pixel clock select	Board-defined	External PLL/oscillator/RAMDAC

Reference Display Modes

Purpose

The following table illustrates common engineering display timings. Exact timing values and maximum pixel clock are determined by the target board and RAMDAC. Modes outside the qualified board list require complete electrical and bandwidth requalification.

Mode	Refresh	Pixel Clock	Stored Format	Status
640 x 480	60-75 Hz	25-32 MHz	8/16/32 bpp	Qualified
800 x 600	60-75 Hz	40-50 MHz	8/16/32 bpp	Qualified
1024 x 768	60-75 Hz	65-80 MHz	8/16/32 bpp	Qualified
1280 x 1024	60-75 Hz	108-135 MHz	8/16/32 bpp	Board dependent
1600 x 1200	60 Hz	~162 MHz	8/16 bpp	Not base-board qualified; representation only

APPLICATION NOTE

Do not infer 1600 x 1200 qualification from timing-register range. Standard VDP-7 evaluation hardware is qualified only to the modes listed in its board documentation.

Hardware Cursor and Color Lookup

Cursor

The scanout cursor supports a maximum 64 x 64 image with transparent states and two programmable direct colors. Cursor movement does not require framebuffer restoration.

Lookup Table

Indexed-color scanout uses an external RAMDAC lookup path controlled through board-level DAC access. Diagnostic software can load ramps to isolate DAC or analog-path faults from drawing faults.

Item	Capability
Cursor size	Up to 64 x 64 pixels
Cursor colors	Two direct colors plus transparent states
Cursor position	Signed screen-relative position
LUT entries	Board/RAMDAC dependent; 256 typical
DAC access	Board-level serial/parallel interface

Interrupts and Status

Interrupt Sources

VDP-7 provides command FIFO, completion, vertical blank, error and diagnostic interrupt sources. Status registers permit polling when interrupts are unavailable or inappropriate.

Error Reporting

Hardware records command decode, framebuffer range, FIFO and selected diagnostic faults. Software should capture status before performing a destructive reset.

Source	Maskable	Typical Use
FIFO_LOW	Yes	Refill command stream
CMD_DONE	Yes	Completion marker
VBANK	Yes	Page flip / synchronization
ERROR	Yes	Fault service
DIAGNOSTIC	Yes	Manufacturing/service tests

Reset and Clocking

Reset Domains

A hardware reset initializes all device domains. Software reset controls permit command-engine recovery while preserving selected display state on qualified board implementations.

Clocking

Core and framebuffer clocks are supplied by the board. Pixel clock is generated by the display clock/RAMDAC subsystem. Clock sequences must meet the startup and stabilization requirements below.

Clock / Reset	Requirement	Notes
RESET#	≥ 10 μ s asserted	After supplies valid
Host clock	25 or 33 MHz	Qualified implementations
Memory clock	40-66 MHz	Board qualified
Pixel clock	Up to 135 MHz base board	External subsystem
Clock stable to access	≥ 1 ms	Before register programming

DC Electrical Characteristics

Conditions

Unless otherwise noted: commercial temperature 0 to 70 °C, VCC = 3.30 V +/- 5%, VIO = 5.00 V +/- 5%. Values are device-pin limits and do not include board regulator tolerance beyond the stated supply range.

Parameter	Min	Typ	Max	Units
VCC core	3.15	3.30	3.45	V
VIO	4.75	5.00	5.25	V
VIH (5 V input)	2.0	-	VIO+0.3	V
VIL	-0.3	-	0.8	V
VOH @ -4 mA	2.4	-	-	V
VOL @ 8 mA	-	-	0.45	V
ICC core active	-	1.8	2.5	A
IIO active	-	0.25	0.40	A

APPLICATION NOTE

Absolute maximum ratings are stress limits only. Functional operation outside the recommended operating conditions is not implied.

AC Characteristics

Timing Reference

AC measurements use 1.5 V switching thresholds for 5 V logic signals unless otherwise specified. Load conditions correspond to the Sinneslöschen evaluation-board reference design.

Parameter	Min	Max	Units	Notes
Host write cycle	30	-	ns	33 MHz qualified host
Host read access	-	42	ns	From select stable
FIFO write recovery	10	-	ns	Between accepted writes
FB memory clock	15.15	25	ns	40-66 MHz
RESET# pulse	10	-	us	Supplies and clocks valid
IRQ assertion delay	-	120	ns	From internal event
VBLANK interrupt delay	-	4	host clocks	Qualified timing

Framebuffer Interface Timing

Interface Model

The external framebuffer interface is synchronous to FB_CLK. Board implementations may use qualified SDRAM or synchronous graphics memory devices with glue logic as required by the reference design.

Signal Integrity

Memory timing margin can be lost through excessive trace mismatch, loading or connector stubs even when static setup calculations appear valid.

Signal Group	Function	Design Guidance
FB_A	Framebuffer address	Route as matched group; avoid unnecessary stubs.
FB_D[63:0]	Framebuffer data	Length-match within byte lanes; maintain controlled impedance.
FB_WE / OE	Memory strobes	Meet board memory setup/hold requirements.
FB_CLK	Memory clock	Low-jitter source; treat as timing reference.
FB_CS	Bank select	Decode delay included in qualification.

Package and Pin Groups

Package

Production VDP-7 devices are supplied in a 208-lead metric quad flat package (MQFP). Pin assignment is organized to separate host, framebuffer and display-control groups while distributing power and ground around the package.

Handling

The device is static sensitive. Use grounded handling procedures and store unmounted devices in approved conductive packaging.

Pin Group	Approx. Pins	Function
VCC / VIO / GND	54	Core/I/O power and return
HOST	52	32-bit host data, address/control
FRAMEBUFFER	78	64-bit data plus address/control/clock
DISPLAY / DAC	12	Timing, DAC control and GPIO
CLOCK / RESET / TEST	12	Clocks, reset, diagnostics

Package Dimensions and Mounting

Mounting

Use the land pattern and soldering profile specified by the Sinneslöschen board-layout guide. Provide uninterrupted ground reference beneath high-activity host and framebuffer signal groups where possible.

Inspection

After reflow, inspect all four lead banks for bridges, lifted leads and incomplete wetting. High-density memory and host groups can exhibit functional faults from a single marginal lead.

Dimension	Nominal	Tolerance
Body size	28.0 x 28.0 mm	+/- 0.20 mm
Lead pitch	0.50 mm	Reference
Lead count	208	-
Overall span	30.6 mm	+/- 0.25 mm
Installed height	3.4 mm max	-
Coplanarity	0.10 mm max	-

Thermal Characteristics

Thermal Design

Active dissipation varies with framebuffer traffic, pixel format and command activity. Provide airflow or local heat spreading where enclosure ambient temperature approaches the upper operating limit.

Industrial Screening

Industrial-temperature devices are supplied only under approved ordering codes and do not make an unqualified board design suitable for the industrial range.

Parameter	Commercial	Industrial
Ambient operating	0 to +70 °C	-40 to +85 °C
Storage	-55 to +125 °C	-55 to +125 °C
Junction max	+125 °C	+125 °C
Theta JA, reference board	~24 °C/W	~24 °C/W
Typical active dissipation	6.8 W	Application dependent

Ordering and Revision Information

Revision Compatibility

Production software should read the REVISION register and use feature bits rather than comparing only ordering-code text. Revision C devices preserve the documented Revision B command model while correcting FIFO watermark behavior.

Traceability

Record device ordering code, lot code, board assembly revision, RAMDAC type and framebuffer memory type when reporting display or timing problems.

Ordering Code	Temperature	Revision / Package
VDP7-BQ-C	0 to +70 °C	B1/B2 production, 208 MQFP
VDP7-BQ-I	-40 to +85 °C	B2 screened, 208 MQFP
VDP7-CQ-C	0 to +70 °C	C1 compatible production
VDP7-CQ-I	-40 to +85 °C	C1 screened, OEM availability

Board-Level Design Guidance

Power Distribution

Use low-impedance planes for VCC, VIO and ground. Place high-frequency decoupling close to each supply group and provide bulk capacitance near the framebuffer and RAMDAC sections.

Host and Memory Routing

Avoid unterminated stubs on host-control and framebuffer-clock nets. Maintain length discipline across the 64-bit framebuffer bus. Treat DAC/pixel-clock routing as an analog-sensitive subsystem.

Bring-Up Sequence

Verify supplies and clocks first, then host register access, revision ID, framebuffer memory test, command FIFO, drawing diagnostics and finally display timing/RAMDAC output.

APPLICATION NOTE

Do not attempt high-resolution display qualification until basic framebuffer integrity and command-engine diagnostics pass at the target operating temperature.

Application Notes and Related Documentation

Required References

Use RM-VDP7-03 for the programming model and register definitions. Use AN-VDP7-05 for high-resolution display design. Use the applicable evaluation-board or system manual for clock/RAMDAC and board-specific qualification limits.

Support

When requesting assistance, provide product ordering code, silicon revision, board assembly revision, framebuffer configuration, display timing, RAMDAC type, operating system/driver version and a captured STATUS/ERROR report.

Document	Title
RM-VDP7-03	VDP-7 Programmer's Reference Manual
AN-VDP7-05	High-Resolution Display Design with the VDP-7
AN-VDP7-06	Framebuffer Bandwidth Planning
SB-97-019	VDP-7 Evaluation Board Power-Up Procedure
RM-GL41-01	Graphics Library 4.1 Programmer's Reference