



Sinneslösch

SYSTEMS CORPORATION

CLEAR SIGNALS. RELIABLE SYSTEMS.

SYSTEMS ENGINEERING

SSB-1 System Bus Technical Reference

Electronic transfer of Revision C source manual

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DOCUMENT STATUS

SCAN INCOMPLETE - This electronic copy contains source pages 1 through 146 only. Appendices B and C (source pages 147-164) have not been transferred to the online Documentation Service.

Notice

This manual defines the electrical, mechanical, timing and service requirements for Sinneslöschen SSB-1 systems. It applies to qualified Sinneslöschen modules and to OEM modules designed under an approved interface agreement.

Safety and Service

- Remove chassis power before installing or removing modules unless the applicable system manual explicitly defines a live-service procedure.
- Observe electrostatic-discharge precautions when handling modules.
- Do not defeat chassis grounding, interlocks or protective covers to obtain bus access.
- Service measurements on powered equipment should be performed only by qualified personnel.

Document Status

Revision C supersedes Revision B. The electronic archive copy is incomplete: Appendices B and C are not included. Contact Documentation Services for information concerning surviving printed copies.

Revision History

Rev.	Date	Description
A	02.14.85	Initial engineering release for SSB-1 chassis and first production module families.
B	09.08.86	Expanded arbitration, interrupt, mechanical and module-design guidance.
C	06.20.88	Revised timing limits, service procedures, power guidance and OEM module qualification requirements.

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Appendices B and C are listed in the source manual but are not present in this electronic transfer.

Preface

SSB-1 was developed to provide a controlled modular interface for industrial systems whose service life could extend well beyond the availability of any single processor or peripheral technology. The bus therefore emphasizes deterministic electrical behavior, documented configuration and field-replaceable modules.

This reference is organized for both system designers and service personnel. Design sections define electrical and timing requirements; installation and service sections describe the procedures required to preserve a qualified configuration after repair or expansion.

System-specific manuals take precedence where they define narrower limits, dedicated address maps or approved exceptions. OEM hardware must not rely on undocumented behavior observed on a single chassis or controller revision.

1. System Bus Overview

Purpose and Scope

SSB-1 defines the electrical, mechanical and service conventions used by Sinneslösch modular control and instrumentation systems introduced beginning in 1985. This reference is intended for system designers, field-service personnel and OEM engineers responsible for qualified SSB-1 installations.

System Property	SSB-1 Definition
Data path	16-bit bidirectional
Address space	24-bit byte address (16 MB)
Transfer type	Asynchronous request/acknowledge
Interrupts	7 vectored priority levels
External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYSCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For purpose and scope, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

SSB-1 System Concept

The bus is a 16-bit asynchronous multidrop backplane with a centralized arbiter, seven vectored interrupt levels and a 24-bit byte address space. Transfer completion is controlled by the selected target through DTACK#, allowing modules with different internal speeds to share one chassis.

System Property	SSB-1 Definition
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Transfer type	Asynchronous request/acknowledge
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External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYSCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For ssb-1 system concept, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

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SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

Chassis and Backplane Organization

Chassis and Backplane Organization is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

System Property	SSB-1 Definition
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1. System Bus Overview

Module Classes

Module Classes is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

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External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For module classes, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

Transfer Philosophy

Transfer Philosophy is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

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Interrupts	7 vectored priority levels
External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For transfer philosophy, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

Long-Service Design Goals

Long-Service Design Goals is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

System Property	SSB-1 Definition
Data path	16-bit bidirectional
Address space	24-bit byte address (16 MB)
Transfer type	Asynchronous request/acknowledge
Interrupts	7 vectored priority levels
External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For long-service design goals, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

System Controller Responsibilities

System Controller Responsibilities is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

System Property	SSB-1 Definition
Data path	16-bit bidirectional
Address space	24-bit byte address (16 MB)
Transfer type	Asynchronous request/acknowledge
Interrupts	7 vectored priority levels
External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For system controller responsibilities, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

1. System Bus Overview

Configuration Records

Configuration Records is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

System Property	SSB-1 Definition
Data path	16-bit bidirectional
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Interrupts	7 vectored priority levels
External masters	Up to 4 request/grant channels
Reference clock	8 MHz SYCLK; not transfer-synchronous
Typical chassis	6U modular card cage, up to 12 slots

For configuration records, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

96-Pin Connector Assignment

Each module uses a three-row 96-contact DIN-style backplane connector. Power and return contacts are distributed to reduce common impedance, while address, data, control, arbitration and interrupt groups are arranged to limit crosstalk between the most active signal classes.

Signal	Class	Description
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For 96-pin connector assignment, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Address and Data Groups

Address and Data Groups is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For address and data groups, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Control Signal Electrical Levels

Control Signal Electrical Levels is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For control signal electrical levels, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Power Distribution

Power Distribution is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For power distribution, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Ground and Return Paths

Ground and Return Paths is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.
SYSCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For ground and return paths, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Signal Loading Limits

Signal Loading Limits is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For signal loading limits, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Backplane Stub Length

Backplane Stub Length is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For backplane stub length, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Termination Networks

Termination Networks is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For termination networks, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Connector Contact Resistance

Connector Contact Resistance is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For connector contact resistance, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Cable/Expansion Restrictions

Cable/Expansion Restrictions is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.
SYSCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For cable/expansion restrictions, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Noise Margin

Noise Margin is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For noise margin, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

2. Electrical and Backplane Definition

Backplane Qualification

Backplane Qualification is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Class	Description
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.



Simplified multidrop backplane. Keep module stubs short and preserve end termination networks.

For backplane qualification, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Read Cycle Sequence

A read begins when the bus master drives a stable address and asserts AS# with RD#. The selected target enables its data drivers only after decode is valid, then asserts DTACK#. The master samples D15-D0 before releasing AS#; the target must remove DTACK# and return its data drivers to high impedance during recovery.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For read cycle sequence, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Write Cycle Sequence

During a write, the master drives address, data and WR# before asserting AS#. The target may latch data at any point after the specified setup interval and must assert DTACK# only when the write can be accepted without violating its local timing. Posted or speculative writes are not part of SSB-1.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For write cycle sequence, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Byte Transfer Cycle

Byte Transfer Cycle is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For byte transfer cycle, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Word Transfer Cycle

Word Transfer Cycle is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For word transfer cycle, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Target Decode Timing

Target Decode Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For target decode timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

DTACK Generation

DTACK Generation is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For dtack generation, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Bus Error Sequence

Bus Error Sequence is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For bus error sequence, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Timeout Behavior

Timeout Behavior is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For timeout behavior, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Slow Peripheral Operation

Slow Peripheral Operation is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For slow peripheral operation, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Back-to-Back Transfers

Back-to-Back Transfers is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For back-to-back transfers, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Bus Turnaround

Bus Turnaround is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For bus turnaround, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

3. Asynchronous Bus Cycles

Cycle Examples

Cycle Examples is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Event	Requirement	Typical
Address valid before AS#	≥ 35 ns	45 ns
Control valid before AS#	≥ 20 ns	30 ns
Target DTACK# after AS#	60-650 ns	180 ns
Read data setup to AS# release	≥ 25 ns	40 ns
Write data hold after AS#	≥ 15 ns	25 ns
Bus recovery	≥ 80 ns	120 ns

For cycle examples, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Arbiter Function

The system controller owns the centralized arbitration function. Up to four external bus masters request ownership with dedicated BREQ#/BGNT# pairs. The controller guarantees that only one external grant is active and inserts a bus-idle interval when ownership changes.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For arbiter function, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Request Levels

Request Levels is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For request levels, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Grant Timing

Grant Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For grant timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Bus Ownership

Bus Ownership is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For bus ownership, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Priority Rules

Priority Rules is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For priority rules, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Fairness and Lockout

Fairness and Lockout is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For fairness and lockout, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Master Release

Master Release is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For master release, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

DMA Controller Use

DMA Controller Use is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For dma controller use, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Multiple Master Example

Multiple Master Example is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For multiple master example, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

4. Centralized Arbitration

Arbitration Faults

Arbitration Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Priority	Request	Use
0	Controller	Highest / system controller
1	BREQ3#	High-priority DMA
2	BREQ2#	Acquisition / disk
3	BREQ1#	General bus master
4	BREQ0#	Lowest external master

For arbitration faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

24-Bit Address Space

SSB-1 addresses 16 MB of byte space. Standard system controllers divide this range into controller-local, memory, I/O and reserved service regions. OEM systems may use different windows, but the installed address map must be preserved in the configuration record.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For 24-bit address space, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Module Base Address

Module Base Address is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For module base address, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

I/O Windows

I/O Windows is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For i/o windows, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Memory Windows

Memory Windows is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For memory windows, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Reserved System Region

Reserved System Region is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For reserved system region, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Configuration Straps

Configuration Straps is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFFh	System controller reserved

For configuration straps, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Address Conflicts

Address Conflicts is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For address conflicts, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Byte/Word Alignment

Byte/Word Alignment is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For byte/word alignment, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Mirrored Decode Hazards

Mirrored Decode Hazards is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For mirrored decode hazards, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

5. Addressing and Mapping

Address Map Worksheet

Address Map Worksheet is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Range	Conventional Use
000000h-0FFFFFFh	Controller/local memory
100000h-BFFFFFFh	System memory / OEM windows
C00000h-EFFFFFFh	Peripheral I/O and shared buffers
F00000h-FFFFFFFh	Service/configuration region
FF0000h-FFFFFFh	System controller reserved

For address map worksheet, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

IRQ Levels

Seven active-low interrupt request lines provide fixed electrical priority from IRQ7# through IRQ1#. A level identifies priority, not a unique module. Systems that share a level require a documented method for identifying the requesting source before service is completed.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For irq levels, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Priority Model

Priority Model is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For priority model, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Vectored Interrupt Cycle

Vectored Interrupt Cycle is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For vectored interrupt cycle, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Interrupt Acknowledge

Interrupt Acknowledge is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For interrupt acknowledge, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Vector Assignment

Vector Assignment is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For vector assignment, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Shared-Level Restrictions

Shared-Level Restrictions is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For shared-level restrictions, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Interrupt Latency

Interrupt Latency is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For interrupt latency, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Service Routine Requirements

Service Routine Requirements is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For service routine requirements, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Spurious Interrupts

Spurious Interrupts is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For spurious interrupts, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

6. Interrupt System

Diagnostic Testing

Diagnostic Testing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

IRQ	Priority	Typical Assignment
IRQ7#	Highest	Critical acquisition / fail-safe
IRQ6#	High	High-rate data source
IRQ5#	High	Mass storage / communications
IRQ4#	Medium	General I/O
IRQ3#	Medium	Serial / timer
IRQ2#	Low	Operator / low-rate I/O
IRQ1#	Lowest	Background service

For diagnostic testing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Module Labels

Module Labels is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For module labels, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Revision Markings

Revision Markings is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For revision markings, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Manual Identification

Manual Identification is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For manual identification, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Configuration Straps

Configuration Straps is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For configuration straps, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Serial/Asset Records

Serial/Asset Records is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For serial/asset records, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Service Configuration Sheet

Service Configuration Sheet is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For service configuration sheet, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Replacement Module Rules

Replacement Module Rules is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For replacement module rules, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

7. Module Identification and Configuration

Configuration Audit

Configuration Audit is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Record Item	Required Entry
Module type	Commercial or OEM designation
Assembly revision	Printed board / assembly Rev.
Serial number	If fitted
Slot position	Physical chassis slot
Address	Base address / strap state
Interrupt	IRQ level and vector
Replacement history	Date and prior module disposition

For configuration audit, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Timing Definitions

Because data transfers are asynchronous, timing limits are specified relative to AS#, RD#/WR#, data validity and DTACK# rather than SYSCLK. SYSCLK is a reference used by selected modules and diagnostics; it does not define the transfer period.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For timing definitions, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Address Setup

Address Setup is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For address setup, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Data Setup/Hold

Data Setup/Hold is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For data setup/hold, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

DTACK Limits

DTACK Limits is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For dtack limits, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Read Recovery

Read Recovery is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For read recovery, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Write Recovery

Write Recovery is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For write recovery, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Bus Master Timing

Bus Master Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For bus master timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Interrupt Timing

Interrupt Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For interrupt timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Arbitration Timing

Arbitration Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For arbitration timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Slow Target Limits

Slow Target Limits is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For slow target limits, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Temperature Margin

Temperature Margin is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For temperature margin, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

8. Timing Requirements

Timing Verification

Timing Verification is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Timing Item	Min	Max	Units
Address setup	35	-	ns
Data setup read	25	-	ns
Data hold write	15	-	ns
DTACK response	60	650	ns
Bus recovery	80	-	ns
Grant to bus use	120	-	ns

For timing verification, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

6U Eurocard Format

Standard SSB-1 modules use a 6U Eurocard mechanical envelope and a 96-contact rear connector. Front-panel dimensions, ejectors and retention hardware vary by chassis family, but the card edge and connector datum must remain within the mechanical limits in this chapter.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For 6u eurocard format, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Card Guides and Retention

Card Guides and Retention is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For card guides and retention, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Connector Mating

Connector Mating is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For connector mating, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

+5 V Distribution

+5 V Distribution is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For +5 v distribution, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

+12/-12 V Auxiliary Power

+12/-12 V Auxiliary Power is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For +12/-12 v auxiliary power, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Current Budgeting

Current Budgeting is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For current budgeting, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Airflow Requirements

Airflow Requirements is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For airflow requirements, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Temperature Range

Temperature Range is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For temperature range, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Shock/Vibration

Shock/Vibration is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For shock/vibration, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

9. Mechanical, Power and Environmental

Chassis Grounding

Chassis Grounding is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Rail	Nominal	Tolerance	Typical Chassis Budget
+5 V	5.0 V	+/-5%	40 A
+12 V	12.0 V	+/-5%	6 A
-12 V	-12.0 V	+/-5%	3 A

For chassis grounding, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Receiving Inspection

Before installation, inspect the chassis for shipping damage, loose hardware, bent card guides and connector contamination. Compare the module inventory against the packing list and system configuration record before applying power.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For receiving inspection, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Chassis Inspection

Chassis Inspection is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For chassis inspection, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Power Supply Checkout

Power Supply Checkout is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For power supply checkout, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Module Inventory

Module Inventory is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For module inventory, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Address/IRQ Setup

Address/IRQ Setup is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For address/irq setup, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Termination Check

Termination Check is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For termination check, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

First Power-Up

First Power-Up is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For first power-up, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Controller Diagnostics

Controller Diagnostics is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For controller diagnostics, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Peripheral Bring-Up

Peripheral Bring-Up is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For peripheral bring-up, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

10. Installation and Commissioning

Commissioning Record

Commissioning Record is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

- Verify chassis part and backplane revision.
- Record every installed module and slot before movement.
- Check termination networks at the physical bus ends.
- Verify supply voltages with modules installed.
- Power up with controller diagnostics enabled.
- Test interrupts and any external bus masters before customer software.

For commissioning record, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Fault Isolation Strategy

Service should proceed from system-level evidence toward the smallest replaceable assembly. Record the failure condition before changing modules. Simultaneous movement of several cards, address straps or termination networks can destroy the information needed to identify the original fault.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For fault isolation strategy, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Power Faults

Power Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For power faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

No DTACK Faults

No DTACK Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For no dtack faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Bus Error Faults

Bus Error Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For bus error faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Address Conflicts

Address Conflicts is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For address conflicts, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Interrupt Faults

Interrupt Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For interrupt faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Arbitration Faults

Arbitration Faults is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For arbitration faults, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Intermittent Errors

Intermittent Errors is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For intermittent errors, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Connector/Backplane Service

Connector/Backplane Service is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For connector/backplane service, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Module Substitution

Module Substitution is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For module substitution, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Oscilloscope Checks

Oscilloscope Checks is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For oscilloscope checks, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

11. Service and Diagnostics

Service Record Completion

Service Record Completion is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Symptom	First Checks
No system activity	Power, RESET#, controller clock, backplane connector
Repeated BERR#	Address conflict, missing DTACK#, target decode
Intermittent data	Connector, termination, loading, marginal timing
Lost interrupts	IRQ wiring, vector conflict, service routine
DMA stalls	Arbitration request/grant, master release, timeout

For service record completion, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Electrical Interface Requirements

A customer-designed SSB-1 module must meet the bus input threshold, output drive, leakage, loading and high-impedance requirements in this manual under worst-case supply and temperature conditions. Passing a room-temperature bench test is not sufficient qualification.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For electrical interface requirements, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Address Decoder Design

Address Decoder Design is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For address decoder design, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

DTACK Circuit Design

DTACK Circuit Design is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For dtack circuit design, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Data Transceivers

Data Transceivers is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For data transceivers, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Interrupt Interface

Interrupt Interface is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For interrupt interface, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Bus Master Interface

Bus Master Interface is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For bus master interface, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Power Decoupling

Power Decoupling is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For power decoupling, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

EMI/Signal Integrity

EMI/Signal Integrity is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For emi/signal integrity, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Connector Pin Usage

Connector Pin Usage is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For connector pin usage, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Prototype Qualification

Prototype Qualification is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For prototype qualification, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Production Test

Production Test is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For production test, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

12. Module Design Guidelines

Documentation Requirements

Documentation Requirements is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Design Check	Requirement
Input loading	Within one standard SSB load per signal unless approved
Output drive	Meet VOL/VOH at full chassis load
Tri-state release	Before bus turnaround limit
Address decode	No overlap outside assigned range
DTACK	Assert only after valid data/write acceptance
Power-up	Outputs high impedance until RESET# release

For documentation requirements, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Signal Summary A-D

This appendix consolidates signal names, direction and active state for field reference. The tables do not replace the detailed electrical and timing requirements in the main chapters.

Signal	Direction / Class	Reference
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.

For signal summary a-d, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Signal Summary E-I

Signal Summary E-I is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.

For signal summary e-i, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Signal Summary J-R

Signal Summary J-R is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.

For signal summary j-r, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Signal Summary S-Z

Signal Summary S-Z is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.
SYSCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.

For signal summary s-z, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Read Cycle Timing

Read Cycle Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.

For read cycle timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Write Cycle Timing

Write Cycle Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.

For write cycle timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Interrupt Acknowledge Timing

Interrupt Acknowledge Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.
SYSClk	Reference	8 MHz reference clock; transfers remain asynchronous.

For interrupt acknowledge timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Arbitration Timing

Arbitration Timing is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
FAIL#	System	System fault/fail indication.
SYSCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.

For arbitration timing, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Electrical Limits

Electrical Limits is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.

For electrical limits, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Loading Tables

Loading Tables is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.

For loading tables, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Termination Values

Termination Values is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.
FAIL#	System	System fault/fail indication.
SYSCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.

For termination values, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Connector Reference

Connector Reference is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
SYCLK	Reference	8 MHz reference clock; transfers remain asynchronous.
A23-A0	Address	24-bit byte address; 16 MB logical space.
D15-D0	Data	16-bit bidirectional data path.
AS#	Control	Address strobe; begins an asynchronous transfer.
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.

For connector reference, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Address Map Reference

Address Map Reference is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
RD#	Control	Read direction indicator.
WR#	Control	Write direction indicator.
BYTE#	Control	Selects 8-bit byte transfer within 16-bit word.
DTACK#	Handshake	Target acknowledges completion of transfer.
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.

For address map reference, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.

Appendix A. Signal and Timing Reference

Service Quick Reference

Service Quick Reference is governed by the SSB-1 compatibility and service philosophy described throughout this manual. The implementation must preserve documented electrical loading, asynchronous handshake behavior, module revision information and the installed system configuration. Changes that appear mechanically simple can alter timing, address ownership or interrupt behavior and therefore require verification before the system is returned to service.

Signal	Direction / Class	Reference
BERR#	Handshake	Target/controller reports bus error or timeout.
BREQ0#-BREQ3#	Arbitration	Bus request lines for up to four external masters.
BGNT0#-BGNT3#	Arbitration	Centralized arbiter grant lines.
IRQ1#-IRQ7#	Interrupt	Seven prioritized vectored interrupt request levels.
IACK#	Interrupt	Interrupt acknowledge cycle indication.
RESET#	System	System-wide bus reset.

For service quick reference, record the installed module revision and chassis backplane revision before changing straps, cabling or module position. The service record is part of the qualified configuration and should be updated after successful verification.

Signal names ending in # are active low. Unless a section explicitly states otherwise, unused control outputs must remain in the inactive high-impedance state and must not be tied directly to a power rail.

Measurements should be made at the receiver or designated backplane test point with a probe whose capacitance does not materially alter the bus waveform. A waveform that changes when the probe is moved can indicate inadequate margin or an excessive stub.

SERVICE NOTE

Do not combine troubleshooting changes. Change one variable, repeat the applicable diagnostic, and record the result before proceeding.